REMARKS

In the Office Action dated April 9, 2003, the Examiner has ***finally rejected*** claims 8, 9, and 13-22 pending in the application on the basis of new ground(s) of rejection and newly cited art. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated April 9, 2003.

A good and sufficient reason why the present response is necessary and was not earlier presented is that an entirely new reference has been cited in the present final rejection date April 9, 2003 (37 CFR §1.116(c)). The new reference is Dalla Liberia et al. (USPN 6,432,762) (hereinafter "Liberia") which is for the first time brought to Applicant's attention by means of the present ***final rejection*** dated April 9, 2003. The new reference, i.e. Liberia, was not cited in the present application prior to the instant final rejection. Since Liberia is a reference upon which the Examiner has now relied, Applicant believes that it would be manifestly unfair for the Patent Office not to consider Applicant's arguments, which are necessitated due to the newly cited reference, Liberia.

The Examiner has rejected claims 8, 9, 13, 17, 18, and 22 under 35 USC §102(e) as being anticipated by Liberia. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 8 and 9, is patentably distinguishable over Liberia. However, Applicant reserves the right to provide declarations and/or documents under 37 CFR 1.131 to "swear behind" the effective filing date of Liberia.

Subject to Applicant's reserved right to establish priority of the present invention under 37 CFR 1.131, Applicant submits that the present invention, as defined by independent claims 8 and 9, includes, among other things, "a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type," and a "gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness." As disclosed in the present application, the present invention provides a thin tunnel oxide layer over a channel region (i.e. the third region) and a thicker tunnel oxide layer over overlap regions (i.e. first and second regions), where the overlap regions and the channel region have an opposite conduction type. As a result, the present invention advantageously achieves a reduced potential for oxide breakdown and/or current leakage in the overlap regions, while providing a suitable injection field for programming and erasing functions in the channel region. Thus, by appropriately controlling the formation of the tunnel oxide layer, the present invention advantageously achieves a memory cell having improved reliability and endurance.

In contrast to the present invention as defined by independent claims 8 and 9, Libera does not teach, disclose, or suggest "a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type," and a "gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said

third region, said first thickness being greater than said second thickness." Libera specifically discloses channel region 31, which is formed in a portion of substrate 10 between region 12 and source region 11. See, for example, column 2, lines 1-4 and Figures 11 and 12 of Libera. In Libera, gate oxide region 18 is situated over channel region 31 and thinner tunnel oxide region 19 is situated over region 12, where channel region 31 and region 12 have opposite conductivity type (i.e. channel region 31 has a P type conductivity and region 12 has an N type conductivity). See, for example, Libera, column 1, lines 40-56.

In Libera, tunnel oxide region 19 is situated between thicker gate oxide region 18 and a portion of gate oxide layer 42, which has a similar thickness as gate oxide region 18 and which is situated over region 12. See, for example, Figures 11 and 12 of Libera. Thus, the above portion of gate oxide layer 42 is situated over region 12 and gate oxide region 18 is situated over channel region 31. However, tunnel oxide region 19 is situated over region 12 and also situated between the portion of gate oxide layer 42 and gate oxide region 18. Thus, in Libera, tunnel oxide region 19 is not situated between thicker gate oxide regions that are situated over regions having a conductivity type that is opposite to the conductivity type of the region that tunnel oxide region 19 is situated over. Furthermore, Libera does not teach, disclose, or suggest a gate insulating layer having a first thickness situated over first and second regions and having a second thickness over a third region, where the first thickness is greater than said second thickness, and where the first and second regions have an opposite conductivity type compared to the third region.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 8 and 9, is not suggested, disclosed, or taught by Libera. As such, the present invention, as defined by independent claims 8 and 9, is patentably distinguishable over Libera. Thus claims 13 and 17 depending from independent claim 8 and claims 18 and 22 depending from independent claim 9 are, *a fortiori*, also patentably distinguishable over Libera for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 14-16 and 19-21 under 35 USC §103(a) as being unpatentable over Libera. As discussed above, independent claims 8 and 9 are patentably distinguishable over Libera. Thus claims 14-16 depending from independent claim 8 and claims 19-21 depending from independent claim 9 are, *a fortiori*, also patentably distinguishable over Libera for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by independent claims 8 and 9, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 8, 9, and 13-22 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance of claims 8, 9, and 13-22 pending in the present application is respectively requested.

Respectfully Submitted,
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Date: 6/9/03

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